DECLARATION

I, the undersigned, of 2-12, Nakazaki 2-chome, Kita-ku, Osaka, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. 10-154700

that was filed in Japanese.

I declare that all statements made herein of my own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

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[Name of the Document] SPECIFICATION

[Title of the Invention] SEMICONDUCTOR DEVICE

[Claims]

[Claim 1] A semiconductor device comprising a bipolar transistor comprising an emitter layer, a base layer and a collector layer, characterised in that

the bipolar transistor has a multi-quantum barrier portion provided in a region of the collector layer in proximity to the base layer and composed of a plurality of barrier layers and well layers alternately stacked to perform the function of reflecting an incident wave of carriers in the collector layer injected from the base layer (minority carriers in the collector layer) and provide such a phase that the incident wave and a reflected wave intensify each other.

[Claim 2] The semiconductor device according to claim 1, characterised in that

the barrier layers and well layers of the multi-quantum barrier portion are composed of respective semiconductor materials having different band gaps.

[Claim 3] The semiconductor device according to claim 1 or 2, characterised in that

a conduction band in the collector layer containing the multi-quantum barrier portion has a band discontinuity value of substantially zero.

[Claim 4] The semiconductor device according to any one of claims 1 to 3, characterised in that

the base layer is strained.

[Claim 5] The semiconductor device according to any one of claims 1 to 4, characterised in that

the base layer is composed of a semiconductor containing at least silicon and germanium.

[Claim 6] The semiconductor device according to claim 5, characterised in that

the multi-quantum barrier portion has a superlattice structure composed of a $Si_{1-x}Ge_x/Si$ multiple layer.

[Claim 7] The semiconductor device according to claim 5, characterised in that

the multi-quantum barrier portion has a superlattice structure composed of a $Si_{1-x-y}Ge_xC_y/Si$ multiple layer.

[Claim 8] The semiconductor device according to any one of claims 1 to 7, characterised in that

the multi-quantum barrier portion is disposed in a region of the collector layer exterior to a depletion region formed between the emitter layer and the base layer at a maximum design voltage when the transistor is operating.

[Claim 9] The semiconductor device according to claim 8, characterised in that

the barrier layer at the end of the multi-quantum barrier portion closer to the base layer is disposed in such a position as to prevent the tunnelling of the carriers from the depletion region formed between the collector layer and the base layer to the well layer adjacent to the barrier layer at the end of the multi-quantum barrier portion closer to the base layer.

[Claim 10] The semiconductor device according to any one

of claims 1 to 9, characterised by further comprising

an element having, as components, two regions having the same structure as a base/collector junction of the bipolar transistor.

[Claim 11] The semiconductor device according to claim 10, characterised in that

the element is a diode.

[Claim 12] The semiconductor device according to any one of claims 1 to 9, characterised in that

the semiconductor device further comprises another bipolar transistor comprising a collector layer disposed in a region used commonly by the base layer of the bipolar transistor, a base layer disposed in a region used commonly by the collector layer of the bipolar transistor, and an emitter layer, and

the semiconductor device functions as an I^2L element.

[Claim 13] The semiconductor device according to claim 12, characterised by further comprising

at least one other collector layer connected to the base layer of the bipolar transistor, and

another multi-quantum barrier portion provided in a region of the one other collector layer in proximity to the base layer and composed of a plurality of barrier layers and well layers alternately stacked to perform the function of reflecting an incident wave of carriers injected from the base layer (minority carriers in the collector layer) and provide such a phase that the incident wave and a reflected wave intensify each other.

[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention relates to a semiconductor device having a heterojunction portion such as a bipolar transistor, a diode or an I^2L element and particularly relates to measures for increase in performance thereof.

[Prior Art]

In a conventional Si LSI using a bipolar transistor, it has frequently been performed to compose a diode by using a PN junction portion between the base and collector of the NPN bipolar transistor and use the diode as an element of a logic circuit. This is because the NPN bipolar transistor has a structure suitable for the formation of a large number of built-in diodes since the PN junction portion between the base and collector has a high breakdown voltage and the N-type collector layer is used as a common region in the substrate.

However, such a PN junction diode has the drawback that it is unsuitable for a high-speed operation. This is because minority carriers are accumulated in each of the P-type and N-type regions of the diode. Specifically, electrons as minority carriers are accumulated in the P-type base layer of the NPN bipolar transistor, while holes as minority carriers are accumulated in the N-type collector layer thereof. In a typical high-speed bipolar transistor, the P-type base layer is formed extremely thin to reduce the base transit time so that the accumulation of the electrons in the base layer presents substantially no problem. However, the collector layer is formed to have a sufficient thickness in the range of 0.5 to 1 μm in order to retain a high breakdown voltage,

so that numerous holes are accumulated therein, which eventually limits the speed of the PN junction diode.

As a method of increasing the operating speed by suppressing the accumulation of minority carriers in such a collector region, there has been known one reported in Document 1 (M. Ugajin et al., "The base-collector heterojunction effect in SiGe-base bipolar transistors," Solid-State Electron., vol.34, pp.593, 1991), in which a SiGe/Si heterojunction is provided at the junction between the base layer and the collector layer to give a wider band gap to the collector layer. By thus giving the wider band gap to the collector layer, a heterojunction barrier is formed in the base/collector junction portion to suppress injection of holes from the base layer to the collector layer, thereby reducing the amount of holes accumulated in the collector layer and increasing the operating speed of the diode.

There has also been known a method disclosed in Document 2 (M. Karlsteen et al., "Improved switch time of I2L at low power consumption by using a SiGe heterojunction bipolar transistor," Solid-State Electron., vol.38, pp.1401, 1995), in which a heterojunction is provided at the junction between the base and the collector in an I^2L (Integrated Injection Logic) circuit into which a plurality of bipolar transistors have been integrated, thereby suppressing the accumulation of minority carriers and increasing the operating speed.

[Problems that the Invention is to solve]

In the conventional bipolar transistor and diode aforementioned, however, there is a limit to the increase of the

operating speed thereof which will be accomplished by providing a heterojunction at the base/collector junction, suppressing injection of minority carriers from the base layer into the collector layer, and thereby reducing the accumulated carriers.

The reason for this is that, as reported in Document 1, a considerably high heterojunction barrier is required to reduce the quantity of holes accumulated in the N-type Si collector layer of a Si/SiGe HBT to the order of the quantity of electrons accumulated in the P-type SiGe base layer thereof. Specifically, a heterojunction barrier of a height on the order of 0.2 eV is required. To form such a heterojunction barrier at the base/collector junction composed of a SiGe/Si multiple layer, the Ge composition ratio in the base layer should be at least 25% or higher.

Meanwhile, it is generally known that a lattice strain develops in a SiGe layer formed by crystal growth on a Si substrate due to the difference in lattice constant between Si and Ge, and is released if the Ge composition ratio is high and the film thickness is large thereby causing a dislocation in the film as well as fatal damage to the element. The film thickness at which a dislocation occurs is generally termed the critical film thickness. The critical film thickness is smaller as the Ge composition ratio in the SiGe layer is higher. The critical film thickness is on the order of 50 nm when the Ge composition ratio is 30%, which corresponds to the film thickness of the base layer.

Even when the film thickness of the SiGe layer is equal to or smaller than the critical film thickness, the SiGe layer is not in a completely stable state but in a quasi-stable state if

the Ge composition ratio is high. If a high-temperature process is performed in a subsequent step, such a defect as dislocation is easily caused. Hence, it is inappropriate in terms of device reliability and a thermal budget during a device fabrication process to use as a base layer a SiGe layer having a high Ge composition ratio.

Therefore, Ge composition ratios of 25% or higher in the SiGe layer are excessively high in terms of reliability and manufacturability. Hence, it is problematic to increase the Ge composition ratio in the SiGe layer in order to increase the height of a heterojunction barrier formed at the base/collector heterojunction.

An object of the present invention is to provide an element functioning as a bipolar transistor, a diode, an I^2L element, or the like which operates at a high speed by suppressing the injection of minority carriers from the base layer into the collector layer and thereby reducing the quantity of minority carriers accumulated in the collector layer. This can be achieved by providing means for effectively increasing a heterojunction barrier formed at the base/collector junction without increasing the Ge composition ratio in the SiGe base layer to such a value as to excessively reduce the critical film thickness, i.e., by implementing a structure which ensures a sufficiently high reliability.

[Means for Solving the Problems]

To solve the above problems, in a semiconductor device according to the present invention, a multi-quantum barrier (MQB), having a superlattice structure consisting of two types of extremely

thin films having different compositions and alternately stacked, is provided in a region of the collector layer closer to the collector/base junction. The height of the heterojunction barrier (barrier height) has been effectively increased by using the effect of reflecting a wave of carriers injected from the base (minority carriers in the collector layer). As a result, the injection of minority carriers from the base layer is suppressed.

The semiconductor device according to the present invention comprises a bipolar transistor comprises an emitter layer, a base layer and a collector layer, and the bipolar transistor has a multi-quantum barrier portion provided in a region of the collector layer in proximity to the base layer and composed of a plurality of barrier layers and well layers alternately stacked to perform the function of reflecting an incident wave of carriers in the collector layer injected from the base layer and provide such a phase that the incident wave and a reflected wave intensify each other.

With this arrangement, the carriers in the base layer are prevented from being injected into the collector layer, not only by a barrier induced by a discontinued valance band at the collector/base junction but also by the multi-quantum barrier portion. By suppressing the injection of minority carriers, therefore, the accumulation of the minority carriers in the collector layer is prevented and the operating speed of a bipolar transistor or the like is increased even if the doping concentration of carriers in the base layer is increased.

In the semiconductor device, the barrier layers and well

layers of the multi-quantum barrier portion are preferably composed of respective semiconductor materials having different band gaps.

This facilitates the implementation of a multi-quantum barrier layer having the function of suppressing injection of minority carriers.

In the semiconductor device, a conduction band in the collector layer preferably has a band discontinuity value of substantially zero.

This provides a band structure presenting no obstacle to the movement of majority carriers in the collector layer, which enhances the effect of improving a current amplification factor.

In the semiconductor device, the base layer is preferably strained.

With this arrangement, a particularly high effect is achieved when the difference in lattice constant between the emitter layer and the base layer is large.

In the semiconductor device, the base layer is preferably composed of a semiconductor containing at least silicon and germanium.

With this arrangement, a heterojunction semiconductor device excellent in RF characteristics can be obtained while using inexpensive semiconductor materials.

In the above heterojunction semiconductor device, the multi-quantum barrier portion may have a superlattice structure composed of a $Si_{1-x}Ge_x/Si$ multiple layer, or may have a superlattice structure composed of a $Si_{1-x-y}Ge_xC_y/Si$ multiple layer.

By composing the multi-quantum barrier portion of a

superlattice structure of a $Si_{1-x-y}Ge_xC_y/Si$ multiple layer, the critical film thickness of the $Si_{1-x-y}Ge_xC_y$ layer at the multi-quantum barrier portion is particularly increased, so that it becomes possible to further increase the effective barrier height of the multi-quantum barrier portion without incurring a dislocation.

In the semiconductor device, the multi-quantum barrier portion is preferably disposed in a region of the collector layer exterior to a depletion region formed between the emitter layer and the base layer at a maximum design voltage when the transistor is operating.

With this arrangement, the function of suppressing injection of minority carriers from the base into the collector can maximally be performed in any operating condition.

In this case, the barrier layer at the end of the multi-quantum barrier portion closer to the base layer is preferably disposed in such a position as to prevent the tunnelling of the carriers from the depletion region formed between the collector layer and the base layer to the well layer adjacent to the barrier layer at the end of the multi-quantum barrier portion closer to the base layer.

With this arrangement, such an improvement in RF characteristics as described above can be expected without degrading the function of suppressing injection of carriers performed by the multi-quantum barrier portion.

The semiconductor device may further comprise an element having, as components, two regions having the same structure as a base/collector junction of the bipolar transistor.

With this arrangement, there can be obtained an element operating at a high speed by using the function of suppressing injection of minority carriers performed by the multi-quantum barrier portion.

The element is, e.g., a diode.

The semiconductor device may further comprise another bipolar transistor comprising a collector layer disposed in a region used commonly by the base layer of the bipolar transistor, a base layer disposed in a region used commonly by the collector layer of the bipolar transistor, and an emitter layer, and the semiconductor device may function as an I^2L element.

With this arrangement, there can be obtained an I^2L element occupying a smaller area and operating at a high speed.

The semiconductor device functioning as the above-mentioned I^2L element may further comprise at least one other collector layer connected to the base layer of the bipolar transistor, and another multi-quantum barrier portion provided in a region of the one other collector layer in proximity to the base layer and composed of a plurality of barrier layers and well layers alternately stacked to perform the function of reflecting an incident wave of carriers injected from the base layer (minority carriers in the collector layer) and provide such a phase that the incident wave and a reflected wave intensify each other.

[Embodiments of the Invention]

The present invention relates to an element such as a heterojunction bipolar transistor, an I^2L element or a diode characterised by having a multi-quantum barrier composed of a

superlattice structure in a region of the collector adjacent the collector/base junction and by effectively increasing the height of a heterojunction barrier (barrier height) through the effect of reflecting carriers thereby suppressing injection of minority carriers from the base layer into the collector layer and reducing the accumulation of the minority carriers in the collector layer, and is directed to the improvement of the operating speed.

Hereinafter, embodiments of the present invention will be described sequentially with reference to the drawings.

(First Embodiment)

Figure 1 is shows a structure of an NPN heterojunction bipolar transistor having a multi-quantum barrier composed of a Si/SiGe superlattice provided in the collector layer according to the present embodiment. As shown in the drawing, a high-concentration n-type Si subcollector layer 2, an n-type Si collector layer 3, a high-concentration p-type SiGe base layer 4, an n-type Si emitter layer 5, and a high-concentration n-type Si emitter contact layer 6 are stacked sequentially on a Si substrate 1 by a UHV-CVD method. A collector electrode 20, a base electrode 21 and an emitter electrode 22 are disposed on the Si subcollector layer 2, the SiGe base layer 4 and the Si emitter contact layer 6, respectively.

A MQB layer 10, as a multi-quantum barrier portion having a superlattice structure composed of extremely thin Si and SiGe films that have been alternately stacked, is provided in a region of the Si collector layer 3 adjacent the collector/base junction portion. The MQB layer 10 has such a structure that the compositions and film thicknesses thereof have been adjusted to reflect an

incident wave of holes injected from the SiGe base layer 4 into the Si collector layer 3 and provide a phase in which the incident wave and a reflected wave intensify each other. Specifically, the MQB layer 10 has a multilayer structure consisting of well layers 10a each composed of a SiGe layer with a thickness of L_1 and barrier layers 10b each composed of a Si layer with a thickness of L_2. The respective thicknesses and compositions of the well layers 10a and the barrier layers 10b are determined to satisfy the relationship represented by the following equation (1).

[Equation 1]

$$\frac{\sqrt{2m_1 * E}}{h} \cdot L_1 = \frac{2m-1}{4}$$

$$\frac{\sqrt{2m_2 * (E-\Delta Ev)}}{h} \cdot L_2 = \frac{2n-1}{4}$$

m_1*: effective mass of holes in SiGe layer (well layer)

m_2*: effective mass of holes in Si layer (barrier layer)

L_1: thickness of SiGe layer (well layer)

L_2: thickness of Si layer (barrier layer)

E: energy of incident holes

ΔEv: valence band discontinuity value at Si/SiGe heterojunction

h: Planck's constant

m, n: integers

Specifically, the MQB layer 10 according to the present embodiment is composed of a superlattice layer consisting of five

pairs of the barrier layers 10b each formed of Si having a thickness of 1.5 nm and the well layers 10a each formed of $Si_{0.8}Ge_{0.2}$ having a thickness of 1.5 nm. In this case, the MQB layer 10 increases an effective barrier height by approximately 130 meV. On the other hand, the SiGe base layer 4 has a graded composition base structure in which a Ge composition ratio increases substantially continually from 0% to 20% from a region closer to the Si emitter layer 5 toward a region closer to the Si collector layer 3. Accordingly, the barrier height sensed by holes in the SiGe layer 4 is 280 meV, which is the sum of 150 meV corresponding to the amount of valence band offset occurring at the base/collector heterojunction composed of $Si/Si_{0.8}Ge_{0.2}$ and 130 meV corresponding to the effectively enhanced barrier height of the MQB layer 10. This achieves a sufficient reduction in the minority carriers accumulated in the Si collector layer 3 through the injection from the SiGe base layer 4.

Figure 2 is a band diagram of the NPN heterojunction bipolar transistor having the multi-quantum barrier composed of the Si/SiGe superlattice and provided in the Si collector layer 3 according to the present embodiment. As shown in the drawing, the multi-quantum barrier consisting of the five pairs of Si barrier layers 10b and $Si_{0.8}Ge_{0.2}$ well layers 10a is provided in the region of the Si collector layer 3 adjacent the collector/base junction. In this arrangement, the effective barrier height sensed by the holes of the SiGe base layer 4 is enhanced by approximately 130 meV. The enhanced effective barrier height suppresses injection of the holes into the Si collector layer 3 even when a hole

concentration in the SiGe base layer 4 is increased, so that the quantity of minority carriers accumulated in the Si collector layer 3 is reduced and the operating speed is increased.

Figure 3 is a diagram showing a model for calculating a barrier height ΔUe enhanced by the MQB layer 10 according to the present invention. The enhanced barrier height ΔUe in each of the five pairs of Si/SiGe superlattice structures composing the MQB layer 10 was calculated for the three structures of $Si/Si_{0.2}Ge_{0.8}$, $Si/Si_{0.3}Ge_{0.7}$ and $Si/Si_{0.4}Ge_{0.6}$. At this time, the respective band discontinuity values ΔEv of the valence bands at the individual heterojunctions between the well layers 10a and the barrier layers 10b are 150 meV, 225 meV and 300 meV. As shown in drawing, the barrier height ΔUe enhanced by the MQB layer 10 is represented at a height virtually formed downward from the valence band of the barrier layer 10b. It is to be noted that the energy level Ec of a conduction band in the whole Si collector layer 3 including the MQB layer 10 is substantially flat and the band discontinuity value in the whole Si collector layer 3 including the MQB layer 10 is substantially zero.

Figure 4 shows the result of calculating the barrier heights ΔUe enhanced by the MQB layer 10 by varying the number of the atomic monolayers of well layers 10a and barrier layers 10b. The calculations were performed by varying x to 0.2, 0.3 and 0.4 in $Si_{1-x}Ge_x$ representing SiGe composing the well layers 10a, i.e., for the three structures of $Si/Si_{0.2}Ge_{0.8}$, $Si/Si_{0.3}Ge_{0.7}$ and $Si/Si_{0.4}Ge_{0.6}$. In the drawing, the abscissa axis represents a well/barrier thickness expressed in the number of atomic monolayers

(one atomic monolayer corresponds to (5.43/4) Å). As shown in the drawing, the enhanced barrier height ΔUe in the MQB layer 10 tends to decrease with an increase in the number of monolayers in any of the cases where x is varied to 0.2, 0.3 and 0.4. The maximum value of the enhanced barrier height ΔUe increases with an increase in Ge composition ratio to reach approximately 240 meV when each of Si and $Si_{0.4}Ge_{0.6}$ of $Si/Si_{0.4}Ge_{0.6}$ is composed of 8 atomic monolayers. When the effective barrier height in the MQB layer 10 is increased by about 240 meV, the function of suppressing injection of holes from the SiGe base layer 4 into the Si collector layer 3 is performed particularly remarkably. Also in the MQB layer 10 using $Si/Si_{0.2}Ge_{0.8}$ not so much likely to be decreased in critical film thickness, the effective barrier height ΔUe becomes a large value of 130 meV or more. This value will be a sufficiently large barrier for suppressing injection of the minority carriers from the SiGe base layer 4 into the Si collector layer 3.

When the barrier height ΔUe is excessively increased in the case where SiGe is used in the well layers 10a of the MQB layer 10, it is necessary to further increase the Ge composition ratio in the well layers 10a. However, the increased Ge composition ratio may cause a dislocation depending on the critical film thickness of SiGe. The respective critical film thicknesses for $Si_{0.2}Ge_{0.8}$, $Si_{0.3}Ge_{0.7}$ and $Si_{0.4}Ge_{0.6}$ when the underlie is Si are approximately 180 nm, 56 nm and 25 nm.

In increasing the critical film thickness, it is effective to use $Si_{1-x-y}Ge_xC_y$ and Si to compose the well layers 10a and barrier

layers 10b of the MQB layer 10, respectively. By adjusting the Ge composition to 40% or more and adding a slight amount of C (on the order of several percentage) thereto, a strained lattice can be alleviated without greatly varying the magnitude of the band discontinuity value ΔEv at the collector/base junction, which increases the critical film thickness of the well layer 10a. By thus composing the MQB layer 10 of $Si_{1-x-y}Ge_xC_y/Si$, a larger band discontinuity value ΔEv can be obtained without exceeding the critical film thickness, which effectively suppresses reverse injection of holes from the SiGe base layer 4 into the emitter layer 5.

By thus providing the MQB layer 10 in the region of the Si collector layer 3 adjacent the base/collector junction of the heterojunction bipolar transistor, it becomes possible to effectively enhance the height of the heterojunction barrier at the base/collector heterojunction and thereby suppress injection of minority carriers from the SiGe base layer 4 into the Si collector layer 3. As a result, the quantity of minority carriers accumulated in the Si collector layer 3 is reduced and the operating speed of the bipolar transistor can be increased.

Although the present embodiment has described the improved characteristics of the heterojunction bipolar transistor as a single element, it will easily be appreciated that the HBT according to the present invention may also be used for the bipolar part of a BiCMOS device in which the bipolar transistor and a CMOS have been integrated.

It will easily be appreciated that, if an integrated circuit

uses as a component the base/collector PN junction of a heterojunction bipolar transistor having a multi-quantum barrier against minority carriers provided in a collector layer, as shown in the present embodiment, the speed of the integrated circuit is increased.

(Second Embodiment)

Figure 5 is a cross-sectional view of an I^2L element comprising a Si/SiGe heterojunction bipolar transistor having a MQB layer provided in a collector layer as shown in the first embodiment. Figure 6 is an electric circuit diagram showing an equivalent circuit of the I^2L element.

A description will be given below to the structure of the I^2L element shown in Figure 5 with reference to Figure 6. The I^2L element according to the present embodiment comprises: an n^+-type semiconductor region 51; an n-type Si common diffusion layer 52 disposed on the semiconductor region 51 to function as the base layer of a PNP bipolar transistor and as the emitter layer of an NPN bipolar transistor; a Si emitter layer 53 and a Si collector layer 54 of the PNP bipolar transistor formed by introducing a p-type impurity into the Si common diffusion layer 52; a p-type SiGe base layer 55 of the I^2L element disposed on the Si common diffusion layer 52; two n-type Si collector layers 56a and 56b of the NPN bipolar transistor disposed on the SiGe base layer 55; an insulating layer 57 covering the entire substrate; two collector electrodes 70a and 70b of the NPN bipolar transistor for contact with the Si collector layers 56a and 56b through the insulating layer 57; a base electrode 71 of the I^2L element for contact with

the SiGe base layer 55 through the insulating layer 57; an injection electrode 72 of the I^2L element for contact with the Si emitter layer 53 of the PNP bipolar transistor through the insulating layer 57; and a ground electrode 73 for contact with the Si common diffusion layer 52 through the insulating layer 57. It is to be noted that the SiGe base layer 55 of the I^2L element functions as the base layer of the NPN bipolar transistor and as the collector contact layer of the PNP bipolar transistor. The I^2L element is structured such that a current for driving the PNP transistor is injected into the injection electrode 72, an input signal to the I^2L element is inputted to the base electrode 71, and an output signal from the I^2L element is obtained from each of the collector electrodes 70a and 70b connected to a power source voltage via an unshown circuit. The arrows shown in Figure 5 represent respective current flows in the PNP and NPN bipolar transistors.

The I^2L element operates as follows. When a low-voltage signal "L" is inputted to the base electrode 71, the current flow in the PNP bipolar transistor becomes as indicated by the solid arrow in the drawing, so that the base voltage of the NPN bipolar transistor is lowered to turn OFF the NPN bipolar transistor. Accordingly, the voltage at each of the collector electrodes 70a and 70b connected to the power-source voltage becomes high so that a signal "H" is outputted. When the high-voltage signal "H" is inputted to the base electrode 71, on the other hand, the current flow in the PNP bipolar transistor becomes as indicated by the dashed arrow so that the base voltage of the NPN bipolar transistor becomes high to turn ON the NPN transistor. As a result, the voltage

at each of the collector electrodes 70a and 70b becomes low so that the signal "L" is outputted. In short, the I^2L element functions as a NOT circuit (inverter).

The I^2L element according to the present embodiment is characterised in that the same MQB layers 60a and 60b as formed in the first embodiment are formed in the two Si collector layers 56a and 56b, respectively.

Such an I^2L element performs the same function as performed by an inverter composed of the PFET and NFET of a CMOS device. Since the I^2L element does not require an isolation film as required by the CMOS device, it has the advantage of suitability to higher integration. However, a conventional I^2L element has the drawback of an elongated time required for ON/OFF switching due to minority carriers accumulated in the collector layer of the NPN bipolar transistor. For this reason, the I^2L element is not frequently used in a semiconductor integrated circuit.

By contrast, since the structure of the I^2L element according to the present embodiment has the MQB layers 60a and 60b provided in the Si collector layers 56a and 56b, respectively, for preventing injection of holes from the base, it is free from the elongated ON/OFF switching time due to holes (minority carriers) accumulated in the Si collector layers 56a and 56b and performs a high-speed operation inherent in a bipolar transistor. Hence, the I^2L element has the advantages of suitability to higher integration and a high-speed operating property, which allows the use of the I^2L element as an inverter in a Si heterojunction device. In addition, power consumption is satisfactorily low compared with the power

consumption of a MOS device.

The I^2L element according to the present embodiment further has the following structural advantages. In contrast to a CMOS device, the NPN bipolar transistor on the output side of the I^2L element has a so-called collector top structure in which the Si collector layers 56a and 56b are disposed above the SiGe base layer 55. The collector top structure is suitable for the provision of the MQB layers 60a and 60b formed by epitaxial growth. More specifically, the I^2L element has the collector top structure in which the collector layer is formed above the base layer because of a plurality of collector outputs, while a normal Si/SiGe HBT generally has an emitter top structure in which an emitter layer is formed above a SiGe base layer formed by epitaxial growth. This is because, in the I^2L element, the emitter and base regions of the NPN bipolar transistor also serve as the base and collector regions of the PNP bipolar transistor as a constant current source, so that the base and collector layers of the NPN transistor are eventually formed by epitaxial growth above the emitter layer.

From this viewpoint, it can also be said that the I^2L element having the MQB layers provided in a region of the collector adjacent the base/collector junction portion of the HBT has an easy-to-fabricate structure.

Although the present embodiment has described the I^2L element using the NPN SiGe HBT, it is also possible to compose the I^2L element by using a PNP SiGe HBT.

The I^2L element according to the present embodiment may be a heterojunction bipolar transistor of a III-V compound

semiconductor.

Although the present embodiment has the two collector layers, it may also have a single collector layer or three or more collector layers.

(Third Embodiment)

A description will be given below to a semiconductor device according to a third embodiment, in which the base/collector junction portion of a bipolar transistor can be used as a diode.

As shown in Figure 7, the semiconductor device according to the present embodiment has a bipolar transistor formation region and a diode formation region. The bipolar transistor formation region and the diode formation region have common members, except for electrodes, which are formed by common process steps. Specifically, there are provided: a Si collector layer 103; a p-type SiGe base layer 104 formed on the Si collector layer 103; an n^+-type Si emitter layer 105 formed on the SiGe base layer 104; an emitter withdrawn electrode 106 composed of polysilicon for contact with the Si emitter layer 105; and a MQB layer 110 formed on a region of the Si collector layer 103 underlying a first exposed region Rexp1, each of which is located in an active region composed of the first and second exposure regions Rexp1 and Rexp2 of the Si substrate 101 surrounded by LOCOS films 102 and of the internal region of the substrate interposed between the exposed regions Rexp1 and Rexp2. A first Si single-crystal film including the Si collector layer 103 is formed by epitaxial growth over the first exposed region Rexp1 and the surrounding LOCOS films, which is thoroughly provided with a superlattice multi-layer structure

common to the MQB layer 110. A p-type impurity has been introduced into the first Si single-crystal film except for the region thereof immediately under the emitter withdrawn electrode 106 by ion implantation using the emitter withdrawn electrode 106 as a mask. The SiGe base layer 104 is formed over the first Si single-crystal film and a second Si single-crystal film is further formed by epitaxial growth over the SiGe base layer 104. The second Si single-crystal film except for the region thereof immediately under the emitter withdrawn electrode 106 forms a silicide layer 108, while the region immediately under the emitter withdrawn electrode 106 forms a Si cap layer 109. The foregoing Si emitter layer 105 has been formed by introducing, by diffusion, a high-concentration n-type impurity into the Si cap layer 109 from the emitter withdrawn electrode 106. A collector withdrawn electrode 111 composed of polysilicon for contact with the Si collector layer 103 is formed over the second exposed region Rexp2 and the surrounding LOCOS films 102. An insulating layer 112 composed of a silicon oxide film is formed on the substrate.

The present embodiment is characterised in that the diode has no electrode equivalent to the emitter electrode, while the NPN bipolar transistor has an Al emitter electrode 115 connected to the emitter withdrawn electrode 106, an Al base electrode 116 connected to the silicide layer provided on the Si base layer 104, and an Al collector electrode 117, each of which is formed on the insulating layer 112. Briefly, only an Al anode 118 equivalent to the base electrode 116 of the NPN bipolar transistor and an Al cathode 119 equivalent to the collector electrode of the NPN

bipolar transistor are provided. Thus, the diode according to the present embodiment has only the anode and the cathode connected to the base and to the collector, respectively, without an electrode connected to the emitter, while having the same emitter, base, and collector structures as the NPN bipolar transistor.

The semiconductor device according to the present embodiment comprises the diode having a heterojunction in addition to the heterojunction bipolar transistor exerting the same effect as exerted in the first embodiment. In the diode also, there is provided a MQB layer 110 in a region of the Si collector layer 103 connected to the cathode electrode 119 adjacent the junction portion between the Si collector layer 103 and the SiGe base layer 104, so that the operating speed is increased by suppressing the accumulation of holes.

[Effects of the Invention]

According to the present invention, a multi-quantum barrier (MQB), composed of a superlattice structure consisting of two types of extremely thin films having different compositions and alternately stacked, is provided in a region of the collector adjacent the collector/base junction, and effectively increases the height of a heterojunction barrier (barrier height) by using the effect of reflecting carriers. Accordingly, injection of the minority carriers from the base layer is suppressed, which suppresses the accumulation of the minority carriers in the collector layer and increases the operating speed.

[Brief Description of the Drawings]

[Fig. 1]

A cross-sectional view of an NPN heterojunction bipolar transistor according to a first embodiment of the present invention, in which a MQB layer as a Si/SiGe multi-quantum barrier portion is provided in a collector layer.

[Fig. 2]

A band diagram of the NPN heterojunction bipolar transistor according to the first embodiment, in which the MQB layer is provided in the collector layer.

[Fig. 3]

A band diagram showing a model for calculating a barrier height ΔUe enhanced by the MQB layer in the transistor of the first embodiment.

[Fig. 4]

A graph showing the result of calculating the barrier height ΔUe enhanced by the MQB layer in the first embodiment.

[Fig. 5]

A cross-sectional view showing the structure of an I^2L element according to a second embodiment, in which a MQB layer is provided in each of two collector layers.

[Fig. 6]

An electric circuit diagram showing an equivalent circuit of the I^2L element according to the second embodiment.

[Fig. 7]

A cross-sectional view of a semiconductor device having a bipolar transistor in which a MQB layer is provided in a collector layer and a diode composed by using only the base and collector of the bipolar transistor.

[Explanation of References]

1	Si substrate
2	Si subcollector layer
3	Si collector layer
4	SiGe base layer
5	Si emitter layer
6	Si emitter contact layer
10	MQB layer
10a	well layer
10b	barrier layer
20	collector electrode
21	base electrode
22	emitter electrode
51	Si substrate
52	Si common diffusion layer
53	Si emitter layer
54	Si collector layer
55	SiGe base layer
56	Si collector layer
57	insulating layer
60	MQB layer
60a	well layer
60b	barrier layer
70	collector electrode
71	base electrode
72	emitter electrode
101	Si substrate

102 LOCOS film

103 Si collector layer

104 SiGe base layer

105 Si emitter layer

106 withdrawn electrode

107 insulating layer

108 silicide layer

109 Si cap layer

110 MQB layer

111 collector withdrawn layer

112 insulating layer

115 Al emitter electrode

116 Al base electrode

117 Al collector electrode

118 Al anode

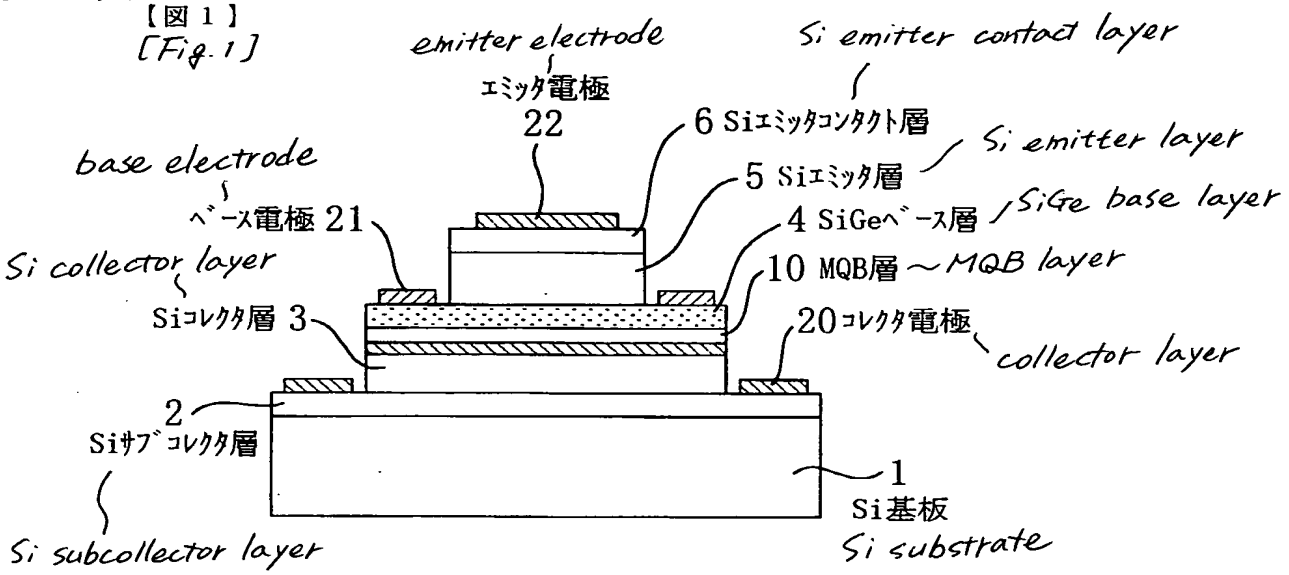
119 Al cathode

Rexp1 first exposed region

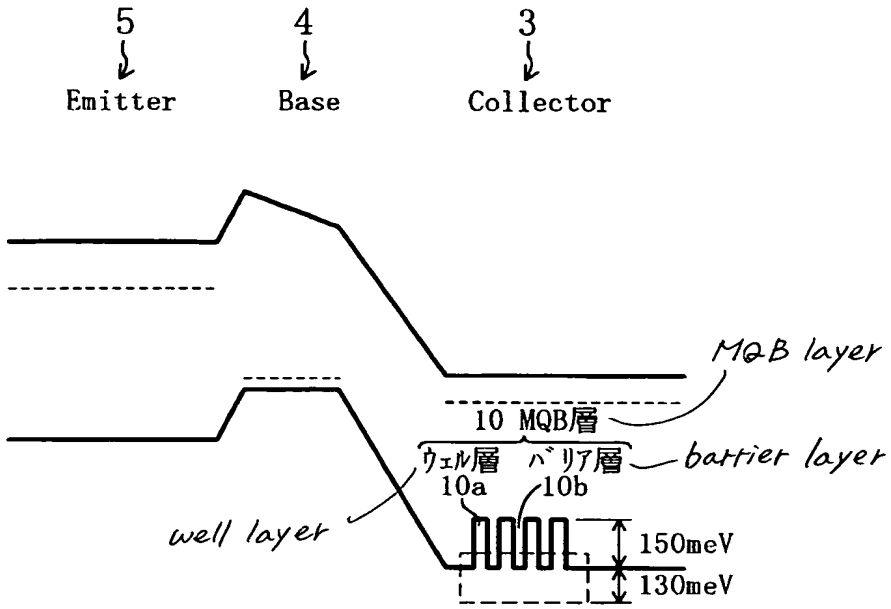
Rexp2 second exposed region

【書類名】　図面
[Name of the Document] DRAWINGS

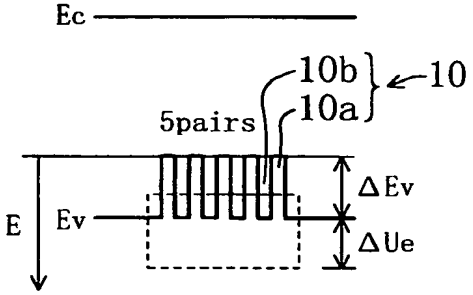
【図１】
[Fig. 1]



【図２】
[Fig. 2]

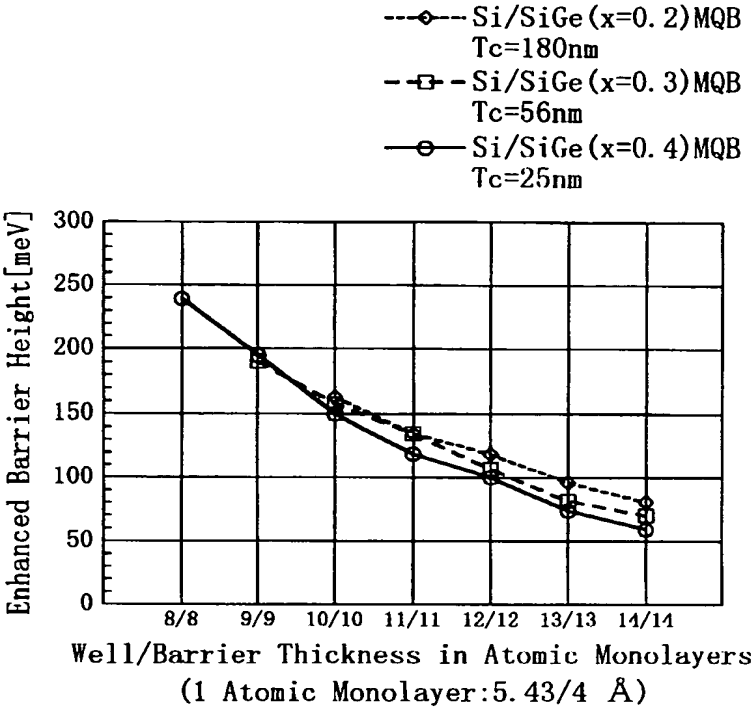


[Fig. 3]
【図３】

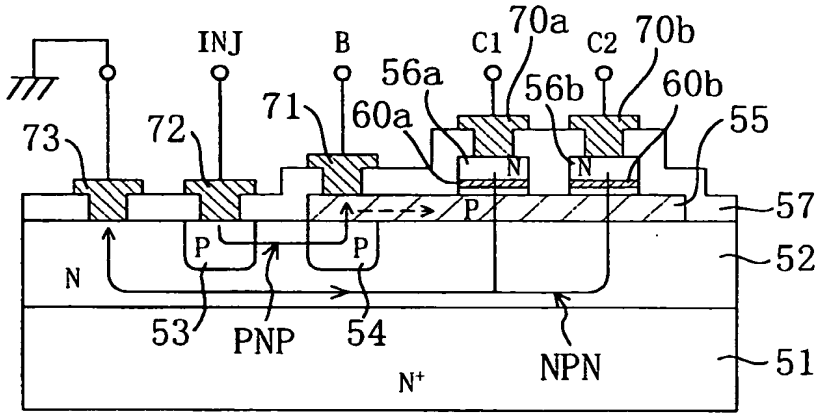


Si/SiGe(x=0.2)　ΔEv=150meV
Si/SiGe(x=0.3)　ΔEv=225meV
Si/SiGe(x=0.4)　ΔEv=300meV

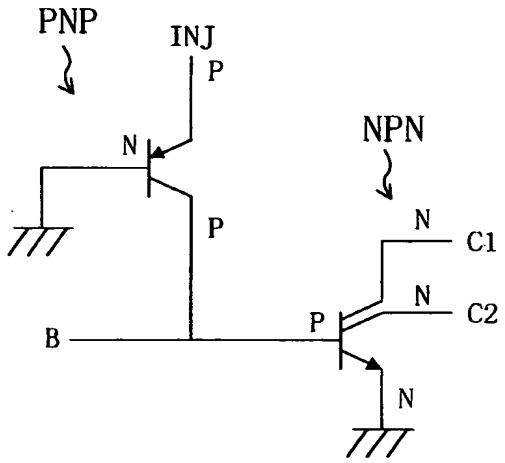
【図４】
[Fig. 4]


Si/SiGe(x=0.2)MQB
Tc=180nm
Si/SiGe(x=0.3)MQB
Tc=56nm
Si/SiGe(x=0.4)MQB
Tc=25nm
Enhanced Barrier Height[meV]
300
250
200
150
100
50
0
8/8
9/9
10/10
11/11
12/12
13/13
14/14
Well/Barrier Thickness in Atomic Monolayers
(1 Atomic Monolayer:5.43/4 Å)

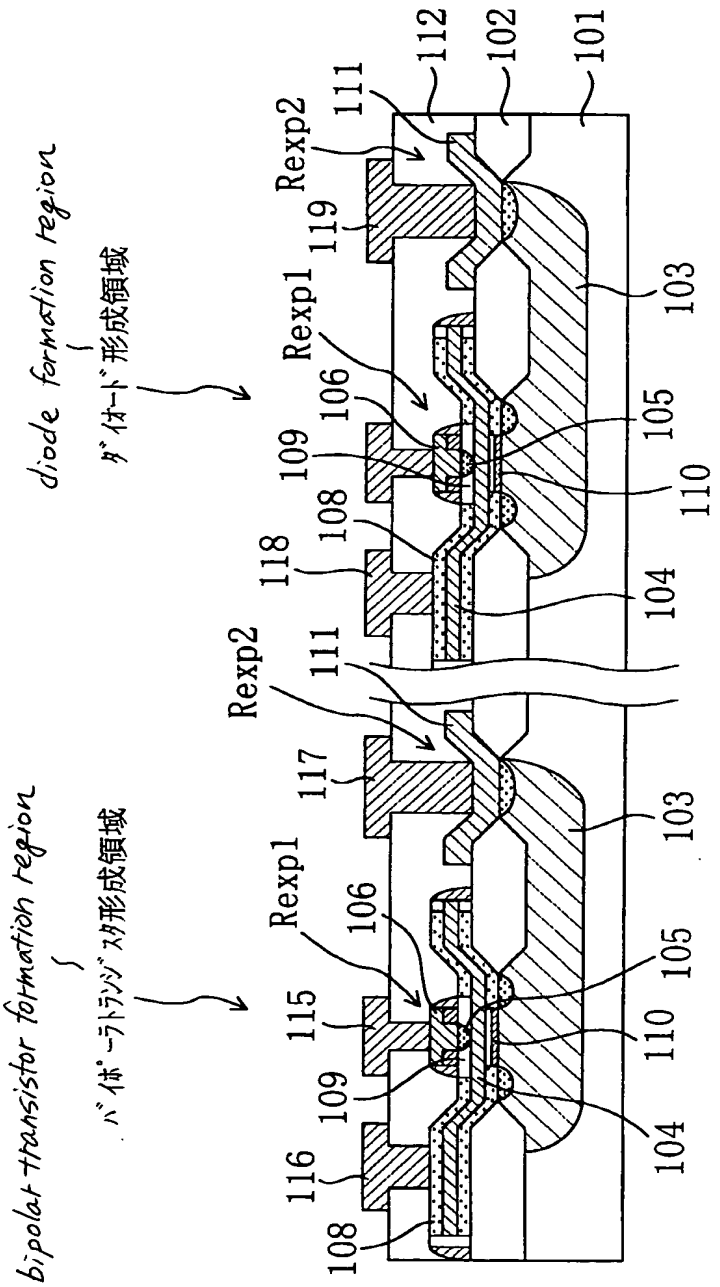
【図５】[Fig. 5]



【図６】[Fig. 6]



【図７】[Fig. 7]


diode formation region
ダイオード形成領域
bipolar transistor formation region
バイポーラトランジスタ形成領域
101
102
103
104
105
106
108
109
110
111
112
115
116
117
118
119
Rexp1
Rexp2

[Name of the Document] ABSTRACT

[Abstract]

[Purpose] To provide a bipolar transistor or a diode which operate at a high speed or an I^2L element excellent in volume production by using a heterojunction of which the function of preventing injection of minority carriers is high.

[Solution] In a region of a Si collector layer 3 adjacent the base/collector junction of a heterojunction bipolar transistor, a MQB layer 10 is provided as a multi-quantum barrier portion composed of a superlattice structure consisting of well layers 10a and barrier layers 10b that are formed of extremely thin films having different compositions and alternately stacked. This enhances an effective barrier height by using the effect of reflecting carriers and thereby suppresses injection of minority carriers from the SiGe base layer 4 into the Si collector layer 3. As a result, the injection of minority carriers can be suppressed by the MQB layer 10, which reduces the quantity of minority carriers accumulated and thereby increases the operating speed.

[Selected Figure] Figure 2